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Item					(5نmrks)	` 	B⊦	I BL BX				
Data bus bits	Item		8085	808	86		General Di	DL DX	T	Da	ta Bus	
Property CISC RISC	Data bus bits	8					1 17	DI		CS	.,	
Memory Segmentation support YES-NO	pipelining					1	397	SI	646	-53		
Max memory space IM64k IM64k IM64k Maximum mode YES-NO YES-NO YES-NO	· · · · · · · · · · · · · · · · · · ·					ALU Dai	ta bus (16 bit)			IP		
Property CISC RISC				100			Tom		Con	nmunication	Control	
Property CISC RISC Clock Cycle(s) per instruction 1 / More than 1 1 / More than 1 microprogramming YES -/ NO YES -/ NO Complexity Higher / Lower Higher / Lower Number of registers More / Less More / Less Code density Higher / Lower Higher / Lower examples μC CPU / GP CPU μC CPU / GP CPU General purpose Q2 b) fill the column 2 of the following table as related to column 1 (7 marks) Registers category Register(s) Computer status register(s) Pointers or offsets or index registers EU registers BIU registers BIU registers Q3-Fill the spaces in the following sentences (14x0.25=4 marks) 2-1. An instruction cycle is as: An instruction located in						100					Logic	
Property CISC RISC Clock Cycle(s) per instruction 1 / More than 1 Execution Unit (EU) Bus Interface Unit (BIU)							The state of the s		Q Bus In	struction que	ue .	
Clock Cycle(s) per instruction	Property		CISC		RISC		(Carried State of Carried State of Carri	System	(8 bit)	2 3 4 5	Tel.	
VES - NO YES - NO	Clock Cycle(s) per instruction	1 / More	than 1	1 / Mo	re than 1							
Number of registers More / Less More / Less	microprogramming .	YES -/ N	10	YES -/	NO '		Executio	1	· bus	interrace	unit (BIU)	
Code density		Higher /	Lower	Higher	/ Lower							
CCPU/GP CPU CCPU/GP CPU GP => general purpose		-									(A)ZOOO	
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THE PROPERTY OF A COLUMN TWO IS NOT THE PROPERTY OF THE PROPER	2-3. The code segments offs	et (effecti	ive address)	is repres	ented by th	ie value i	n (_) register.	If this off	set = (A6	3F)h and CS	

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age	to the following table, choose	se from item 2 that matches item 1. (14x0.5-7 marks)					
U	11(11)	Item 2	<u>^</u>				
1	Interface	transfers data between RAM and I/O without having to go through CPU					
2	The 8086 processor	can supports 256 different interrupts					
3	PIC 8259	Can work with other CPU in the same system					
1	If interrupt occurs	1 chip contains group of jichips that are designed to work with 1 or more related functions					
5	Multi Core processor	a controller used to manage the timing between computer devices					
5	8086 in maximum mode	More than 1 processor in a single chip					
7	PIT-8253/8254	Input/output ports are treated by CPU as RAM locations					
3	PPI 8255	A data structure with FILO data access mechanism					
)	Stack	Auto set to 1 if arithmetic operation result <1					
10	Sign Flag, SF	Controls the interface between CPU and I/O ports					
11	Chipset	Automatically CPU pushes the flags and the next instruction address in the stack					
2	DMA controller 8257	Controls the interrupts priority					
13	Memory mapped I/O	electronic circuits that make the computer compatible with the peripherals					
14	Instruction cycle	programmable interval timer controller	(Servi				
			70				
5-	Choose the right answer	(20x0.5 = 10 marks)					
3-1	. CPU architecture using micropi	rogramming makes it	0 (1)				
2)	more complex architecture	b)more expensive c)more efficient d) more integrated e) all	f) non of all				
3-2	 A μP is capable of addressing a 	1M Bytes of memory if it supports					
	a) 8 bit data bus and 20 b						
	c) 20bit address bus and						
3-3	 Program counter is incremented a) before finishing of execution 	on of current instruction b) after linishing of execution of current instruction					
	c) after fetching of current ins	truction d)at same time e)All f) none of	the all				
3-	1. in 8086 the physical address is	computed by a)BIU b) EU c) ALU d)KAM	ENDAMA Dell				
3-:	Segmentation is applied to a)	registers b) RAM c)ROM d) ALU c)data bus f)CPU g)Address bus	h)DMA i)all				
3-	6. In segmentation, segments	b) code segment must be larger d)could be same or di	fferent size				
	a) should be same size	O and a call	17741				
_	d) data segment must be la 7. Program Counter (PC) represe		000				
3-	a)physical Address In AL	b) Effective Address in RAM c) physical Address in Digital Address in	ME61616				
	d)physical Address in RA	M e)Effective Address in ALU f)Effective address in stack	~\W <i>E\\</i> /\\				
3	-8. the most flexible addressing	mode that can be changed in run time is	OFFEE				
	a) -agistar b)in	nmediate c)indirect register c)indirect memory					
3-	9. The way of how the addressing	of source and destination in an instruction is called b)addressing mode d)bus mode e)execution mode					
	a) data mode In an assembly instruction formation	of the first fields is the a) source of data b)destination of data	c)operation co				
	d)Segment name	e)directives f) immediate data g) data addressing mode h)n	on of all				
3-11	. Which of the flowing instruction	on is the fastest? a) add cx,dx b) add bx,cx c) add ax,bx d) add bx,ax	e)add ax,ax r addressing mode				
3-12	. Which of the following cause:	s RAM access if it is used a) indirect register addressing mode b) register	r addressing mode				
	c) Immediate addressing n	node up.					
3-	13. Instruction pipelining system						
	 a) faster single instruction c) faster hardware access 	d) faster program counter e) all f) not of	all				
3-14. In 8086, which of the following registers which is used as loop counter?							
a) CX b) BX c) AX d) DX e) DI 1) DS							
3-15. In 8086 supports maximum segment size of locations (bytes) of memory							
(20bytes -64 bytes- 4k8k16k20K32k64k128k256k512k1M2M1G2G20G)							
	, -		of all				
1	a)control unit b)ALU	cyregisters dyramit					
3-17. In assembly language programming, directives are used to tell a) user what to b) programmer what to do c) processor what to do							
	d) assembler what to do	c)all D none of all					
3.	-18. PPI 8255 is used as interface		RAM				
	-19. PIT 8253/8254	the first state and dating	and is it is				
	a) generates peripheral clock						
	c) used as Sync/Async. trans	Sinite and receive					
3	-20. DMA controller; used to trans		以上分类性				
	at training to a 4.4 and 4 to	ANA or I/O and DAM ninciveen ALU mid KAIVI	AND RESIDENCE OF THE PARTY OF T				
	 a) between RAM and R c) between CPU and R 	N 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	II.				

Q.6. Assume that a CPU uses instructions pipelining for three inst	ructions, each instruction segmented to live suges
1. Fetch (F)	(ଧୂମିରର
2. Decode (D 3. Execute (E)	[WZ//{{/}/
4. Read (R),	VIII
5 11/20 (11/2)	latancy = 0 and all instructions are completely independen
By assuming that each stage takes 1 Clock Cycle(CC), 1CC = 2ns, 1 do the following:	(Total 7 marks)
(a)use sketching to show pipelining mechanism) (1 marks)	ΛΠΛΩΩ
b) calculate the time needed to finish the overall process of execution of	of the 3 instructions using
(i) sequential (1 marks)	(45/4/4)
(ii) pipelining (1 marks) (c) calculate the process throughput (instruction/s) in both cases, seque	ntial and pipelining - (1 mark)
(d) using your results calculate the speedup in this process. (1 ma	ırk)
(e)by assuming CC=2ns, latency = 0 and all instructions are completely	independent, if process has 1000 instructions each of 5
stages	
(i) if the time needed to finish a process of n instructions each of k :	stages is (k+(n-1) CC calculate the time needed to
finish a process of 1000 pipelined instructions each of 5 stages (1	mark)
(ii) calculate the time of 1000 sequential instruction (1 mark)	
O 7 hair flag and the fellowing	(7lin)
Q.7- briefly answer the following a) What 8086 minimum and maximum modes mean?, (1 mark)	(7 marks)
b) Referring to 8086 pins and signals shown in Fig. 1, list down the	
corresponding signals if minimum mode is used (use table below	v) (2marks)
Pin Min Mode Max Mode number signal signal	
number signal signal	

	MAX /MIN)
	MODE (MODE)
	GND $1 \qquad 40 U_{cc}$
the state of the s	AD14 0 2 39 AD15
	AD13 4513 135 135 136 A16/SS 135 135 135 135
c) State the name and function of each chip shown in Fig.2 (4 marks)	AD12 4 6 37 A17/54
	AD11 5 35 A18/S5
	AD10 5 35 A19/S6
-CS 1 28 VCC PA2 2 39 PAS 070 24 VCC	AD9 7 34 D SRE/S7
$A \stackrel{\text{VR}}{\rightarrow} A \stackrel{\text{Z7}}{\rightarrow} A \stackrel{\text{A0}}{\rightarrow} \stackrel{\text{PA0}}{\rightarrow} 4 \qquad B \qquad 37 \stackrel{\text{PA5}}{\rightarrow} \qquad 60 \stackrel{\text{Q2}}{\rightarrow} \qquad 23 \stackrel{\text{R}}{\rightarrow} \qquad 1$	ADB B 33 MN/MX
	AD7 9 32 日和
06 5 24 IR6 GND 7 34 DO 04 14 21 \overline{\text{CS D6}} \	ADS 10 (PJ 31 RQ/CTO (HOLD)
04 1 Intel 22 First 1977 32 F02 M/6 19740	ADS 1: 30 RQ/GTI (-LDA)
D3 8 8759 21 R3 PC6 11 8255A 30 D4 01 07 8/33 18 DQK2	AD4 12 29 LOCK (NR)
D2 9 20 IR2 PC4 13 28 D6 00 8 17 D0 7 2 D7 0 X 0 Q X 0	ADJ 1 13 28 1 S2 (V/10);
00 11 18 180 PC2 16 26 VCC 010 15 15 10 K4	AD2 14 27 5. OTĀ)
AS 1 4 13 16 4 - 5P/-EN PBO 4 18 23 12 PBS OAL 0 4 11 14 4 GALET	26 H 20 (DBN)
GND 14 15 CAS 2 PB1 19 22 PB4 GND 12 13 DOUT 1	ADO 16 25 QSC (A.E)
	NMI 0 17 24 0 QS: (NTA)
o으므므닷티를 삼노큐토斯틱	NTR
CSD AND STATE OF A CONTRACT OF	CLK 19 22 REACY
	GND 20 21 RESET
D 8257	
	Fig. 1
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